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This book constitutes the refereed proceedings of the 10th International Workshop on Power and Timing Modeling, Optimization and Simulation, PATMOS 2000, held in Göttingen, Germany in September 2000. The 33 revised full papers presented were carefully reviewed and selected for inclusion in the book. The papers are organized in sections on RTL power modeling, power estimation and optimization, system-level design, transistor level design, asynchronous circuit design, power efficient technologies, design of multimedia processing applications, adiabatic design and arithmetic modules, and analog-digital circuit modeling.

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